REMARKS

Claims 1 - 9 are pending and under consideration in the above-identified application.

In the Office Action, Claims 1 - 9 were rejected, and Figures 1 - 5 and 7 - 8 were objected to.

In this Amendment, Claims 2, 5 and 9 have been amended, and Claims 1, 3, 4, and 7 - 8 have been cancelled. No new matter has been introduced as a result of this Amendment.

Accordingly, Claims 2, 5 - 6 and 9 are at issue.

I. Objection to the Specification

The disclosure has been objected to because of informalities.

As requested, Applicants submit that the Specification has been amended in the sections identified by the Examiner, and respectfully request that the objection to the specification be withdrawn.

II. Objection to the Drawings

Figures 1 - 5 and 7 - 8 were objected to.

In reply, Applicants have amended the figures at issue and submitted corresponding Replacement Sheets.

Accordingly, Applicants respectfully request that the drawing objection be withdrawn.

III. 35 U.S.C. § 102 Anticipation Rejection of Claims

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Nakamura (JP Publication 2003-230055).

The rejection of Claim 1 is now moot in view of its cancellation. Accordingly, Applicants respectfully request that this claim rejection be withdrawn.

IV. 35 U.S.C. § 103 Obviousness Rejection of Claims

Claims 2 - 5, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura in view of Hashimoto (U.S. Patent 5,288,988).

Although Applicants respectfully traverse this claim rejection, Claim 2 has been amended to clarify the invention and remove any ambiguities that may have been at the basis of this claim rejections.

Claim 2 is directed to a solid state imaging device with a unit pixel.

In relevant part, Claim 2 recites:

> "...a photoelectric converter for generating a charge in accordance with an amount of incident light;
> a transfer transistor for transferring a signal of the photoelectric converter to a floating node;
> an amplifier transistor for outputting a signal of the floating node to a signal line,
> a reset transistor for resetting the floating node, at least one of a plurality of potentials supplied to a gate electrode of the reset transistor being a negative potential; and
> a portion able to supply three or more types of potentials to the gate electrode of the reset transistor,
> wherein,
> the device has a portion able to set the gate potential when bringing the reset transistor from an On state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential.

That is, the device has a portion able to set the gate potential when bringing the reset transistor from an On state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential. This amendment is supported in at least paragraphs [0052] - [0059] of the instant application published as US Publication 2007/0024726 on February 1, 2007, as appended below:

> [0052] In the present embodiment, by driving the reset transistor 14 by three values (or four values or more) through the drain line 23, the V-shift register 25 provides a potential difference between potentials of the floating nodes ND11 in the selected row and the nonselected row and clarifies the operations in the two selected row and nonselected row.
> [0053] For example, in the present embodiment, one of the potentials supplied to the gate electrode of the reset transistor 14 is at least the negative potential.
> [0054] Further, for example, the V-shift register 25 supplies a voltage of at least one type of potential among at least three types of potentials supplied to the gate electrode of the reset transistor 14 as the negative potential.
> [0055] Further, the V-shift register 25 can set the gate potential when changing the reset transistor 14 from the ON state to the OFF state at the negative power source

potential after passing through the ground level power source potential from the positive high level power source potential.

[0056] Further, in the present embodiment, at both timings of sampling and holding of the precharge phase and the data phase, the gate potential of the reset transistor 14 is set at the ground potential.

[0057] Further, the V-shift register 25 makes the gate potential of the reset transistor 14 in the nonselected pixel at the negative potential in the period during which the gate potential of the reset transistor 14 in the selected pixel is set at the ground potential.

[0058] The drive operation of this reset transistor 14 will be explained in further detail later.

[0059] At one side of the vertical direction (up/down direction in the figure) of the pixel area, for each column, a load transistor 27 configured by an N-type MOS transistor is connected between one end of the vertical signal line 22 and the ground. This load transistor 27 functions as a constant current source when connected at its gate to a load line 28.

This is clearly unlike Nakamura and Hashimoto, taken singly or in combination with each other.

The Examiner acknowledges that Nakamura fails to disclose a portion able to supply three or more type of potentials to the gate electrode of the reset transistor, but advances that Hashimoto allegedly does and points to the reset transistor M of Figure 1, for support. However, Hashimoto states in column 3, lines 59 - 65, that (emphasis added):

> "*The positive pulse of Φ12 firmly turns off the FETs M, so that the base voltage level is not influenced by the ground connection through the FETs M during read-out.* Subsequently, the column shift register turns on the FETs 8 in turn to read out the signals from the storage capacitors 5 to the common horizontal output line 7 and the amplifier 9."

Thus, Hashimoto fails to teach or suggest a portion able to set the gate potential when bringing the reset transistor from an On state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential, as required by Claim 2.

As such, Claim 2 is patentable over Nakamura and Hashimoto, taken singly or in combination with each other, as is dependent Claim 5, for at least the same reasons.

Independent 9, amended to recite the same distinguishable limitation as that of Claim 2, is also patentable over Nakamura in view of Hashimoto.

Accordingly, Applicants respectfully request that this claim rejection be withdrawn.

V. 35 U.S.C. § 103 Obviousness Rejection of Claim

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura in view of Hashimoto and further in view of Mabuchi (JP 2000-092392).

Claim 6 is indirectly dependent on Claim 2, shown above to be patentable over Nakamura in view of Hashimoto.

Moreover, in addition to Nakamura and Hashimoto, Mabuchi also fails to teach or suggest a portion able to set the gate potential when bringing the reset transistor from an On state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential, as required by Claim 2.

As such, Claim 2 is patentable over the three references, taken singly or in combination with each other, as is dependent Claim 6, for at least the same reasons.

Accordingly, Applicants respectfully request that the claim rejection be withdrawn.

VI. 35 U.S.C. § 103 Obviousness Rejection of Claim

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura in view of Nakamura et al. (US Patent 6,873,034) ("Nakamura '034").

The rejection of Claim 7 is now moot in view of its cancellation.

Accordingly, Applicants respectfully request that the claim rejection be withdrawn.

VII. Conclusion

In view of the above amendments and remarks, Applicant submits that Claims 2, 5, 6 and 9 are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

If the claims are not found to be in condition for allowance, the Examiner is requested to contact the undersigned to schedule an interview before the mailing of the Office Action. Any communication initiated by this paragraph should be deemed an Applicant initiated interview.

Respectfully submitted,

Dated: March 9, 2009

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